REMARKS

These remarks are in response to the Office Action dated March 26, 2008 (Office Action). As this reply is timely filed, no fee is believed due. Claim 1 has been amended. No new matter has been introduced. Claims 1-20 and 22 remain pending.

Applicant continues to proceed with the understanding that the citation of U.S. Patent No. 5,409,661 was a typographical error. Applicant presumes that U.S. Patent No. 5,408,661 to Kuranaga (Kuranaga) was the intended citation.

Rejections under 35 U.S.C. § 112

On page 2 of the Office Action, in noting that the 35 U.S.C. § 101 rejection has been overcome, the Office Action states that 35 U.S.C. § 112 issues have arisen. On page 3, however, the Office Action indicates that the rejections under 35 U.S.C. § 112 have been withdrawn. Applicant presumes that the 35 U.S.C. § 112 rejections have been overcome and that no other rejections are outstanding other than those under 35 U.S.C. § 103(a) below.

Rejections Under 35 U.S.C. § 103(a)

Claims 1-20 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,981,153 to Pang et al. (Pang) in view of U.S. Patent No. 6,496,971 to Lesea et al. (Lesea). Applicant presumes that claims 1-18, 20, and 22 stand rejected under 35 U.S.C. § 103(a) in view of the combination of Pang and Lesea.

Regarding claim 1, the Office Action concedes that Pang does not disclose "a microcontroller within the PLD (programmable logic device) for receiving an encrypted bitstream". Still, the Office Action contends that Pang discloses other aspects of claim 1 that involve the microcontroller. For example, the Office Action asserts that Pang discloses a key storage register coupled to the microcontroller for storing key data. While Pang discloses a register for storing key data, that register is not coupled to a microcontroller residing within the PLD. Similarly, the Office Action asserts that Pang discloses "a configuration data register in the PLD, wherein the configuration data register cannot be read by the microcontroller after the decryptor is used." Since Pang

does not disclose a microcontroller, Pang cannot teach or suggest a configuration data register as recited in claim 1. The suggestion that Pang discloses the features noted above, while also conceding that a microcontroller within the PLD receiving an encrypted bitstream is not shown, ignores the plain meaning of claim 1 and infers functionality within Pang that does not exist.

Claim 1 further recites "wherein only the decryptor reads from the key storage register". In FIG. 3, Pang clearly illustrates the key memory 23 being connected to both a decryptor 24 via bus 28 and JTAG logic 13 via bus 25. In describing FIG. 3, in column 7, lines 45-48, Pang states "[b]us 25 carries data, addresses, and control signals to perform write and read operations and allows programming of the decryption keys from JTAG port 20." At column 16, lines 19-25, Pang again discusses the use of bus 25 to write values to and read values from key registers. In these passages, Pang teaches the opposite of that which is recited in claim 1. That is, Pang teaches away from claim 1 since Pang states that both the JTAG port and the decryptor can read the decryption keys, whereas claim 1 recites that only the decryptor reads from the key storage register.

Lesea has been cited for teaching that a PLD includes a microcontroller that receives an encrypted data stream. The Office Action cites column 4, lines 12-25, which reference "decoding circuitry 13." The decoding circuitry 13, however, is an address decoder for the microprocessor and is labeled as such in FIG. 3. Column 7, lines 20-30 describe the functionality of the address decoder 13. As known, an address decoder determines the particular area in memory from which data is read or to which data is written. The cited portion of Lesea is unrelated to encryption or providing an encrypted data stream to a microcontroller within a PLD. Contrary to the position taken by the Office Action, Lesea does not disclose a microcontroller within the PLD that receives an encrypted bitstream.

Claim 4 recites "wherein the decryptor is a software decryptor stored in a memory and executed by the microcontroller, wherein the system further comprises hardware that selectively enables access to the key storage register by allowing the microcontroller access when a program counter of the microcontroller specifies an address within an address range corresponding to the software decryptor within the

memory." The Office Action contends that Pang teaches this feature at column 20, lines 27-53 and that Lesea teaches this feature in columns 40-53.

Applicant will address Pang first and then turn to Lesea. As noted, the Office Action has conceded that Pang does not disclose a microcontroller receiving an encrypted bitstream. Since claim 4 is directed to selectively allowing access of the microcontroller to the key storage register according to a value of the program counter (program counter of the microcontroller), it is not conceivable that Pang discloses this feature. Indeed, the passage of Pang cited by the Office Action is directed to reading the bitstream that is loaded into the PLD to determine whether that bitstream is encrypted. Pang does not mention that access by the microcontroller to a key storage register is selectively enabled according to a value stored in the program counter of the microcontroller.

Turning to Lesea, Applicant presumes that the Office Action intends to refer to columns 4-5, since columns 40-53 do not exist within the Lesea specification. Columns 4-5 discuss how the PLD is able to select one of two different configuration modes for programming the PLD according to a mode code supplied to input/output block (IOB) terminals of the PLD. Here, Lesea does not disclose that the microcontroller is utilized in performing encryption and/or decryption. Rather, Lesea discloses that either the first or second configuration mode, for configuring the PLD, is selected according to the code that is read at the IOB terminals of the PLD. Lesea does not disclose that the value of a program counter is utilized to determine whether the microcontroller is provided access to the key register. Suggesting that Lesea does disclose these features changes the principle of operation of Lesea since Lesea does not disclose encryption and/or decryption of a bitstream. As noted, the decoding circuitry of Lesea cited by the Office Action is a memory address decoder, not decryption circuitry.

Claims 9, 12, and 20 recite one or more features which have been addressed above. These claims are believed to be allowable over the combination of Pang and Lesea. The remaining claims rejected under the combination of Pang and Lesea also are believed to be allowable in view of their own merits and further by virtue of their dependence upon underlying base claims discussed above.

In sum, the combination of Pang and Lesea does not render Applicant's claims obvious. Modifying Pang to incorporate the microcontroller of Lesea would change the principle of operation of Pang. For example, at least in one instance noted above, Pang teaches the opposite of that which is claimed. Further, the Office Action contends that because Lesea discloses a microcontroller, that microcontroller can be inserted into Pang. This line of reasoning ignores the functionality and interoperability recited in Applicant's claims between the key storage register, the decryptor, the configuration data register, and the microcontroller. Simply including the microcontroller would not provide this functionality, particularly where Pang includes teachings that oppose, or teach away from Applicant's claims. Moreover, as Applicant has noted, Lesea does not disclose a microcontroller receiving an encrypted bitstream as asserted by the Office Action. In view of the above, withdrawal of the 35 U.S.C. § 103(a) rejection of claims 1-18, 20, and 22 is respectfully requested.

Claims 1-20 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pang and Lesea in view of U.S. Patent No. 5,409,661 to Kuranaga (Kuranaga). Applicant presumes that the Office Action intended to reject only claim 19 has under 35 U.S.C. § 103(a) in view of the combination of Pang, Lesea, and Kuranaga. Claim 19 is believed to be allowable in view of its own merits as well as the deficiencies of both Pang and Lesea discussed above. Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejection of claim 19 is respectfully requested.

Formalities

Claims 1, 3, 7 and 8 have been further amended to more particularly point out and distinctly claim the subject matter. To wit, Applicant has amended "Programmable Logic Device (PLD)" to reflect a more correct integrated circuit having programmable logic. These amendments are supported at least in paragraph [0005] of the present Application. No new matter is, therefore, added by entry of these amendments.

CONCLUSION

Claims 1, 3, 7 and 8 have been amended herein. Claim was previously cancelled. All claims are now in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being filed via EFS-Web with the United States Patent and Trademark Office on June 13, 2008.

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